What Is Claimed Is:

1. An integrated circuit, comprising:

a sleep switch, provided between a first power supply line and a second power supply line, which is constituted by a transistor of a first threshold voltage, and which becomes non-conducting in a sleep mode;

a latch circuit, connected to said second power supply line , which is constituted by a transistor of a second threshold voltage which is lower than said first threshold voltage;

a ferroelectric capacitor for storing data held in said latch circuit in accordance with polarization direction of a ferroelectric film thereof; and

a control signal generating circuit which, when returning to an active mode from said sleep mode, generates a plate signal for driving a terminal of said ferroelectric capacitor to generate a voltage in said latch circuit in accordance with the polarization direction, and generates a sleep signal for causing said sleep switch to conduct to thereby activate said latch circuit following the driving of said ferroelectric capacitor.

2. An integrated circuit comprising:

a sleep switch, provided between a first power supply line and a second power supply line, which is constituted by a transistor of a first threshold voltage, and which becomes non-conducting in a sleep mode, the first and second power supply

lines and the sleep switch being provided on each of a high power supply line side and a low power supply line side:

a latch circuit, connected to the second power supply line on said high power supply line side and the second power line on said low power supply line side, which is constituted by a transistor of a second threshold voltage which is lower than said first threshold voltage;

a ferroelectric capacitor for storing data held in said latch circuit in accordance with polarization direction of a ferroelectric film thereof; and

a control signal generating circuit which, when returning to an active mode from said sleep mode, generates a plate signal for driving a terminal of said ferroelectric capacitor to generate a voltage in said latch circuit in accordance with the polarization direction, and generates a sleep signal for causing the pair of sleep switches on said high power supply line side and low power supply line side to conduct to thereby activate said latch circuit following the driving of said ferroelectric capacitor.

3. The integrated circuit according to Claim 1 or Claim 2, wherein said ferroelectric capacitor comprises at least a pair of ferroelectric capacitors, one terminal of each ferroelectric capacitor being connected respectively to a pair of storage terminals of said latch circuit, and

said plate signal is supplied to the other terminal of said ferroelectric capacitors such that a voltage in

accordance with the polarization direction of said ferroelectric capacitors is generated in the pair of storage terminals of said latch circuit.

4. The integrated circuit according to Claim 1 or Claim 2, wherein said ferroelectric capacitor comprises two pairs of ferroelectric capacitors, one terminal of each ferroelectric capacitor being connected respectively to the pair of storage terminals of said latch circuit, and

the other terminals of one of the ferroelectric capacitors of the ferroelectric capacitor pair connected to each storage terminal of said latch circuit are driven by a plate signal such that a voltage in accordance with the polarization direction of the ferroelectric capacitor pair connected to each storage terminal is generated in the pair of storage terminals of said latch circuit respectively.

5. The integrated circuit according to Claim 3, wherein said plate signal is supplied to the other terminal of said ferroelectric capacitor when said sleep mode is entered such that said ferroelectric capacitor is set in a predetermined state of polarization in accordance with the voltage level of the pair of storage terminals of said latch circuit.

6. The integrated circuit according to Claim 4, wherein said plate signal is supplied to the other terminal of said ferroelectric capacitor pair when said sleep mode is entered

such that said ferroelectric capacitor pair is set in a predetermined state of polarization in accordance with the voltage level of the pair of storage terminals of said latch circuit.

7. The integrated circuit according to Claim 1 or Claim 2, further comprising a switch circuit, provided between said ferroelectric capacitor and said latch circuit, which enters a conducting state when said active mode is returned to from said sleep mode and enters a non-conducting state during active mode.

8. The integrated circuit according to Claim 7, wherein when said active mode is returned to from said sleep mode, said switch circuit conducts to connect between said latch circuit and said ferroelectric capacitor.

9. The integrated circuit according to Claim 1 or Claim 2, further comprising a reset circuit, provided on one terminal of said ferroelectric capacitor, which enters a conducting state when said active mode is returned to from said sleep mode, to reset the level of said one terminal of said ferroelectric capacitor to a predetermined level.

10. The integrated circuit according to Claim 9, wherein said one terminal enters a floating state following resetting by said reset circuit, whereupon said plate signal is supplied.

11. The integrated circuit according to Claim 9, wherein said reset circuit enters a conducting state when said sleep mode is moved to from said active mode such that the level of said one terminal of said ferroelectric capacitor is reset to a predetermined level.

12. The integrated circuit according to Claim 1, further comprising:

a nonvolatile region having a nonvolatile latch circuit including said latch circuit and said ferroelectric capacitor; and

a volatile region having a volatile latch circuit including said latch circuit but not annexed with said ferroelectric capacitor,

wherein a clock which halts during said sleep mode is supplied to the latch circuit of said nonvolatile region.

13. The integrated circuit according to Claim 1, further comprising:

a nonvolatile region having a nonvolatile latch circuit including said latch circuit and said ferroelectric capacitor; and

a volatile region having a volatile latch circuit including said latch circuit but not annexed with said ferroelectric capacitor,

wherein each latch circuit of said nonvolatile

region is provided with a clock gate circuit for supplying a clock in accordance with a sleep mode control signal.

14. The integrated circuit according to Claim 1, further comprising:

a plurality of circuit blocks,

wherein each circuit block is respectively provided with said sleep switch, said latch circuit, said ferroelectric capacitor, and said control signal generating circuit, and further comprising:

a power supply management circuit for supplying sleep mode control signals respectively to said control signal generating circuits.

15. The integrated circuit according to Claim 1, wherein said latch circuits and the ferroelectric capacitors annexed thereto are disposed in dispersed locations, and said plate signal is supplied to these dispersed ferroelectric capacitors.

16. The integrated circuit according to Claim 1, wherein said latch circuits and the ferroelectric capacitors annexed thereto are disposed in concentration, and said control signal generating circuit is disposed close to the concentrated latch circuit group and ferroelectric capacitor group.

17. The integrated circuit according to Claim 1, wherein said ferroelectric capacitor comprises a real capacitor for

storing the storage terminal level of said latch circuit according to the polarization direction, and dummy capacitors disposed on the periphery of the real capacitor.

18. An integrated circuit comprising:

a sleep switch, provided between a first power line and a second power line, which is constituted by a transistor of a first threshold voltage, and which becomes non-conducting in a sleep mode;

a latch circuit, connected to said second power line, which is constituted by a transistor of a second threshold voltage which is lower than said first threshold voltage;

a combinational circuit, connected to said second power line, which is constituted by a transistor of said second threshold voltage;

a nonvolatile data holding circuit for storing data held by said latch circuit during said sleep mode; and

a control signal generating circuit which, when returning to an active mode from said sleep mode, generates a recall signal for generating a voltage in said latch circuit in accordance with the state of said nonvolatile data holding circuit, and thereafter generates a sleep signal for causing said sleep switch to conduct to thereby activate said latch circuit.